A Hybrid Design Framework for Fast Transient and Voltage Balancing in a Three-level Flying Capacitor Boost Converter with Digital Current Mode Control

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Abstract—Multilevel flying capacitor boost (MLFCB) dc-dc converters offer high power density even at high voltage gain, in which digital control can achieve fast transient and high efficiency. However, the challenges remain in identifying simple yet useful analysis and design techniques to ensure stability and flying capacitor (FC) voltage balance under uniform sampling. This paper proposes a hybrid framework for stability analysis and controller design in an MLFCB converter under digital current mode control (DCMC). Continuous-time (CT) small-signal models (SSMs) of an MLFCB converter are derived, which seem to closely resemble the SSMs of a traditional boost converter. Thereafter, a novel DCMC architecture is proposed, consisting of a Type-II (output voltage) digital controller and a proportional FC voltage controller. With a slower FC voltage loop, the Type-II controller is designed using the CT SSM, which fails to predict fast-scale instability while aiming for higher closed-loop bandwidth. After that, a discrete-time (DT) modeling framework is developed, and the model accuracy is verified using SIMPLIS switch simulation. Using DT SSSMs, closed-loop stability analysis is carried out, and the digital Type-II controller gains are further tuned to achieve fast transient performance with stability. A 100 W, 12/48 V three-level flying capacitor boost (3LFCB) converter prototype is developed, and the proposed DCMC is implemented using an FPGA device. Transient performance and stability are demonstrated using experimental results, which are found to be consistent with the analytical predictions.

Index Terms—Multilevel, flying capacitor, boost converter, digital control, current mode control, continuous-time, discrete-time modeling, fast-scale, stability, analysis, controller design.

I. INTRODUCTION

Multilevel flying capacitor boost (MLFCB) dc-dc converters offer high power density with a high voltage gain, which has been gaining increasing adoption in emerging applications, such as photovoltaic and fuel cell-based renewable system, automotive, data center, to name a few [1]–[6]. This is primarily because of reduced device voltage stress, which enables one to operate at a higher switching frequency even at a higher voltage gain with reduced switching losses. While retaining the same voltage gain as a traditional boost converter, the inductor size can be much smaller in an MLFCB converter for the same ripple current specification [6], because of higher effective switching frequency using FCs. This can achieve higher power density with substantially reduced right-half-plane (RHP) zero effect, which results in significantly improved start-up and transient performance. However, the closed-loop bandwidth is still limited by the RHP zero [7], due to the indirect power transfer nature.

Under DCMC, the choice of modulation techniques and its effect on the RHP zero have been studied in a boost converter [8]–[10], where interval-2 sampling is shown to be useful in reducing the RHP zero effect to some extent. However, it is difficult to achieve the control bandwidth beyond $1/3$rd of the RHP zero frequency [11]. A nonlinear control method using a geometric tuning approach has been proposed in [12], [13], to improve the performance beyond the small-signal performance limit, particularly in the presence of the RHP zero in a boost converter. However, the same analysis can not be extended to this converter because of additional FC dynamics.

The presence of FCs in the MLFCB converters requires suitable strategies for voltage balancing for stable periodic behavior [7], [14]–[21]. A natural balancing has been reported in [16], which requires complex model information. Also, the current balancing aspect during parallel operations has not been investigated. In [17], the natural balancing was achieved using extra passive elements, which would tend to degrade the efficiency and power density. Phase shift modulation techniques were reported in [18], [19]; however, the suitability of this approach is limited to multilevel inverters, which was not explored in high-frequency dc-dc converters. The technique in [20] can achieve FC balancing without using extra sensing circuitry; however, the use of clamping circuits would result in more losses with an increased number of FC stages. A voltage mode control (VMC) based active balancing method was reported in [7]; however, this technique may not be suitable for parallel operation without any external current balancing algorithms. In majority of FC voltage balancing, CT modeling techniques are generally used to predict the effect of parameter variations. However, for digital control, the effects of controller gains and sampling delays are crucial, which have not been considered so far for DCMC architectures.

A peak current mode control (CMC) architecture has been reported in [22], [23] for the FC voltage balancing, and a CT stability analysis has been presented in [24] for peak and valley CMC. CT modeling approaches have been extensively used to design the controller parameters in [7], [14], [20], [21] for the 3LFCB converter. A variable frequency method was reported in [21] to balance the FC voltage throughout the duty range. In the majority of available methods, the effects due to RHP zero, FC voltage loop controller gain, and sampling delay of a DCMC 3LFCB converter, have not been investigated so far.

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CT modeling approaches are useful because they provide design insight in terms of output impedance and other important transfer functions. However, such techniques are insufficient to predict fast-scale instability in digitally controlled 3LFCB converters. A DT modeling technique is useful, which has been extensively used in digitally controlled DC-DC converters [25]–[32]. However, it is difficult to derive accurate DT models because of the structural changes in the state space models due to the reconfiguration in the FC dynamics.

This paper aims to develop a unified discrete-time (DT) modeling framework in a 3LFCB converter to accurately capture the closed loop dynamics under DCMC. Thereafter, a hybrid design framework is introduced for analysis and digital controller design by utilizing the simplicity of the CT approach and the accuracy of the DT approach in a digitally controlled 3LFCB converter which is shown in Fig. 1. Thereafter, a novel DCMC architecture is proposed for fast transient and FC voltage balancing. Controller design guidelines are presented, and root locus plots are obtained to identify stability boundaries for varying controller gains and sampling delays.

This paper is organized as follows. In Section II, a new digital CMC architecture is proposed for active FC voltage balancing with fast transient response in a 3LFCB converter. Section III presents modeling techniques, more specifically, the development of a unified DT modeling framework. A hybrid design framework is proposed in Section IV for controller design and close-loop stability analysis. Section V presents the hardware implementation and experimental performance of the 3LFCB converter using the proposed DCMC technique. Section VI concludes the paper.

II. THE PROPOSED DIGITAL CURRENT MODE CONTROL

Fig. 2 shows the proposed digital current mode control architecture in a 3LFCB converter in Fig. 1.

A. Working principle and timing diagram

The proposed method considers a mixed-signal implementation consisting of an analog current loop and digital voltage loops for the output voltage and FC voltage controllers. The sensed output voltage and FC voltage are digitized using a time-multiplexed analog-to-digital converter (ADC). The outputs of the digital voltage controllers are converted into the analog current references using a time-multiplexed DAC as shown in Fig. 2. Thereafter, the gate signals for the MOSFET drivers are generated using a trailing-edge PWM technique.

A Type-II compensator, \( G_c(z) \) is used for the output voltage controller to generate the current reference \( i_{ref1} \), whereas a simple proportional gain is used as the FC voltage controller, \( G_{cf}(z) \). The output of \( G_{cf}(z) \) is subtracted from the output of \( G_c(z) \) to generate the current reference \( i_{ref2} \). These references, along with the respective ramp compensations, are used to derive the gates signals for the respective switches \( S_2 \) and \( S_1 \) as shown in Fig. 2.

Two current references are considered, which are reconfigured within a switching cycle for comparison with the sensed inductor current of the 3LFCB converter to ensure FC voltage balancing as shown in Fig. 3. The output voltage \( v_o \) and FC voltage \( v_f \) are sampled during mode-3 configuration. A small time delay of 200 ns is considered between the sampling edges of \( v_o \) and \( v_f \), which is negligible compared to the switching period of 10 \( \mu s \). The sampling clock \( F_s \) is considered in synchronization with the fixed-frequency switching clock \( f_{s1} \) along with a delay of \( t_{s1} \) to account for the ADC conversion and controller computation times. Another clock \( f_{s2} \) is derived by delaying \( f_{s1} \) with a time delay \( T/2 \). The clocks \( f_{s1} \) and

![Fig. 1: Circuit diagram of the 3LFCB converter with non-idealties](image1)

![Fig. 2: Block diagram of proposed DCMC architecture in 3LFCB converter](image2)

![Fig. 3: Modes of operation and timing diagram under DCMC for \( D > 0.5 \)](image3)
are used to turn on $S_2$ and $S_1$, respectively. The control references $v_{c1}$ and $v_{c2}$ are time-multiplexed for comparison with the inductor current $i_{L,n}$ using an analog comparator. The rising edges of the comparator outputs $u_{c1}$ and $u_{c2}$ are used to turn off $S_2$ and $S_1$ using R-S flip flops as shown in Fig. 2.

B. Proposed FC voltage balancing mechanism

$$V_f = \frac{0.5V_o}{L}$$

$$V_f < 0.5V_o$$

$$i_{ref1}$$

$$i_{ref2}$$

$$V_f = 0.5V_o$$

Fig. 4: FC voltage balancing mechanism with proposed DCMC scheme

For $D > 0.5$, the sequence of modes of the 3LFCB converter under the proposed digital controller is shown in Fig. 3. The figure shows that the flying-capacitor $C_f$ is charged and discharged during mode 2 and mode 3, respectively, which is disconnected from the power circuit during mode 1. Fig. 4 presents the waveform related to an active FC balancing technique using two reconfigurable current references $i_{ref1}$ and $i_{ref2}$. The balancing technique automatically adjusts the current references using a proportional voltage controller if the FC voltage $V_f$ deviates from $V_o/2$. A smaller gain is considered to slow down the FC voltage loop in order to avoid interactions with the fast-changing output voltage loop. Thus, the FC voltage takes time to reach steady-state during transients; however, it has insignificant impacts on the control bandwidth of the primary voltage controller.

C. Inner current loop stability

A fixed frequency peak CMC technique usually suffers from inner current loop instability [11]. Fig. 5 shows the control waveform of a peak current mode controlled 3LFCB converter. Neglecting the current path gain and sampling delays, the inductor current samples $i_{L,n}$ and $i_{L,n+1}$ under two successive sampling instances in Fig. 5 can be written as

$$i_{L,n} = (i_{ref,n} - i_{cf,n}) - m_{x1}t_{x1}$$

$$i_{ref,n} = (i_{ref,n} - i_{cf,n}) - m_{x1}t_{y1} + m_{x2}t_{x2}$$

$$(1)$$

Putting the time intervals given in Fig. 5 in (1), the inductor current at $(n+1)^{th}$ sample can be evaluated as

$$i_{L,n+1} = i_{ref,n} - m_{y2}T + \frac{m_{y2}}{m_{x2}}\left[\left(1 + \frac{m_{y1}}{m_{x1}}\right)icf, n\right]$$

$$- \left(\frac{m_{y1}}{m_{x1}}\right)icf, n + \left(\frac{m_{y1}}{m_{x1}}\right)i_{L,n} + \left(\frac{m_{x1} + m_{y1}}{2}\right)T$$

$$(2)$$

The small-signal dynamics of (2) after perturbation can be expressed in digital domain as

$$i_L(z) = \left(1 - M_x\right)z^{-t_{ef}(z)} + \left(M_y + M_x\right)z^{-t_{ef}(z)}$$

$$(3)$$

where, $M_x = (m_{y1}m_{y2})/(m_{x1}m_{x2})$ and $M_y = m_{y2}/m_{x2}$

For the inner current loop stability requirements, the eigenvalues of the equation (3) must remain within the unit circle, i.e., $|M_x| < 1$. Thus, the inner current loop is stable $\forall D \in \{(0, 0.25) \cup (0.5, 0.75)\}$. In this work, the steady state duty is somewhat higher than 0.75; thus, the soft transition is considered to ensure current loop stability [11].

III. THE PROPOSED DISCRETE-TIME MODELING OF 3LFCB UNDER DIGITAL CURRENT MODE CONTROL

A. Approximate CT model

Considering the converter states as $x = [x_1 \ x_2 \ x_3]^T$, with inductor current as $x_1$, FC voltage as $x_2$, and output capacitor voltage as $x_3$, the state space model of 3LFCB converter in Fig. 1 can be written as

$$\dot{x}(t) = A_{q1q2}x(t) + Bv_{in}$$

$$v_o = C_{q1q2}x(t); \quad v_f = E_{q1q2}x(t)$$

$$(4)$$

where,

$$A_{q1q2} = \begin{bmatrix} \frac{p}{L} & \frac{q_1-q_2}{L} & -\frac{q_2}{L} \\ \frac{q_2}{C_f} & 0 & -\frac{\alpha}{RC_o} \\ \frac{q_2}{C_o} & 0 & -\frac{\alpha}{RC_o} \end{bmatrix}; \quad B = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$

$$C_{q1q2} = \begin{bmatrix} \frac{q_2}{RC_f} & 0 & \alpha \end{bmatrix}; \quad E_{q1q2} = \begin{bmatrix} (q_2 - q_1)R_C \\ 0 \\ 1 \end{bmatrix}$$

where, $p = -((r_L + 2r_{on}) + \alpha R_C q_2) + (v_C(q_1 q_2 + q_1)))/L$. Here $q_1$ and $q_2$ represent the gate signals for the respective switches $S_1$ and $S_2$ with ‘1’ as the ON state and ‘0’ as the OFF state, and $\alpha = R/(R + r_C)$. A state-space averaging method is applied to obtain the small-signal CT model [33]. The FC charging and discharging intervals are identical at steady-state; thus, the FC dynamics may not appear in the small-signal models. Thereafter, neglecting slower FC dynamics, the...
control-to-output transfer function (TF) \( G_{vc} \), under peak CMC, can be approximated and derived using a similar approach in a boost converter [11], which is derived as

\[
G_{vc}(s) = \left. \frac{\hat{v}_c}{\hat{v}_{in}} \right|_{\hat{v}_{in} = \hat{i}_c = 0} = k_g \left( 1 - \frac{s}{\omega_{hp}} \right) \left( 1 + \frac{s}{\omega_z} \right) \left( 1 + \frac{s}{\omega_p} \right)
\]  

(5)

where,

\[
k_g = \frac{RD'}{2H_i} \omega_{hp} = \frac{RD'^2}{L}, \quad \omega_z = \frac{1}{r_C C_o}, \quad \omega_p = \frac{2}{(R + 2r_C)C_o}.
\]

\( H_i \) is the current sense gain, which is used to scale the current reference into an equivalent voltage reference as \( \hat{v}_c = \hat{i}_{ref} H_i \).

![Fig. 6: A comparative study of frequency response of the control-to-output TF in a current mode controlled 3LFCB converter](image)

Frequency response of the TF in (5) is compared with that obtained using SIMPLIS simulation in a CMC 3LFCB converter, which is shown in Fig. 6. The figure shows that while the magnitude plots are consistent, the phase plots deviate considerably with increasing frequency. Thus, while providing physical insight in terms of pole/zero, the approximate CT model in (5) may not be sufficient to predict fast-scale instability. Also, the FC dynamics cannot be captured; thus, it is essential to develop accurate DT models.

### B. The proposed DT large-signal modeling

A 3LFCB converter undergoes mode reconfigurations with structural changes in the state space dimension, consisting of five modes for \( D > 0.5 \) as shown in Fig. 7. A sampling delay is also considered. A generic DT large signal model can be analytically derived for the 3LFCB converter. A generic solution of the state vector in (4) can be obtained as [25]

\[
x(t) = e^{A_{q_1 q_2} (t-t_0)} x(t_0) + \Gamma_{q_1 q_2} (t-t_0) B v_{in};
\]

(6)

where,

\[
\Gamma_{q_1 q_2} (t) = \left\{ \begin{array}{ll}
(e^{A_{q_1 q_2} (t)} - I) A_{q_1 q_2}^{-1} & \text{if } A_{q_1 q_2} \text{ is nonsingular} \\
\sum_{j=1}^{\infty} A_{q_1 q_2}^{-1} \frac{t^j}{j!} & \text{if } A_{q_1 q_2} \text{ is singular}
\end{array} \right.
\]

\[
x_{n+1} = \left[ \begin{array}{c}
\sum_{i=1}^{p-1} \left( \prod_{j=0}^{i-1} e^{A_{Q_p-j} t_{f_p-j}} \right) (I + \Gamma_{Q_p} (t_p))
\end{array} \right] B v_{in} + \left( \prod_{j=0}^{p-1} e^{A_{Q_p-j} t_{f_p-j}} \right) x_n = f_1(x_n, d_1, d_2)
\]

(7)

where, \( Q_k \) defines mode \((q_1 q_2)\) at \( k^{th}\) interval of operation.

### C. Validation of DT large-signal model

The large signal model of the 3LFCB converter obtained in (7) is validated with SIMPLIS simulation at 100 V input for a duty ratio of 0.75, which is shown in Fig. 8. A model validation case study is demonstrated for a step change in load resistance from 320 \( \Omega \) to 160 \( \Omega \). The figure shows that the DT large signal model is capable of accurately capturing steady-state and dynamic behavior at every sampling instant of the time domain simulation results for varying load resistance.

![Fig. 7: Periodic evolution of a 3LFCB converter within a sampling period, \( T_s \) with \( A_{Q_{k+1}} \) and \( C_{Q_{k+1}} \) correspond to system, input, and output matrices](image)

![Fig. 8: Large signal model verification of the 3LFCB dc-dc converter using SIMPLIS switch simulation and the DT model](image)

### D. DT small-signal modeling

The DT small-signal model can be obtained from the DT large-signal model in (7) by applying the Jacobian linearization around an operating point, which can be written as [25]

\[
\dot{x}_{n+1} = \left. \frac{\partial f_1}{\partial x_n} \right|_{SS} x_n + \left. \frac{\partial f_1}{\partial d_1} \right|_{SS} \dot{d}_1 + \left. \frac{\partial f_1}{\partial d_2} \right|_{SS} \dot{d}_2
\]

(8)

where the co-efficients \( A_{eq} \), \( B_{eq1} \) and \( B_{eq2} \) are defined in Table II. The control-to-output TF for the digital CMC can be
TABLE II: System matrix and input matrix of the small signal model in (8) and (11)

<table>
<thead>
<tr>
<th>$A_{eq}$</th>
<th>$e^{A_{eq}(D_2 T_{-t_2} - t_2)} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} e^{A_{eq}(D_1 - 0.5) T} e^{A_{eq} D_2 T}$</th>
</tr>
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<tbody>
<tr>
<td>$B_{eq1}$</td>
<td>$e^{A_{eq} D_2 T_{-t_2}} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} (A_{eq} - A_{01}) T e^{A_{eq}(D_1 - 0.5) T}$</td>
</tr>
<tr>
<td>$B_{eq2}$</td>
<td>$e^{A_{eq} D_2 T_{-t_2}} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} (A_{eq} - A_{01}) T e^{A_{eq}(D_1 - 0.5) T}$</td>
</tr>
<tr>
<td>$B_m$</td>
<td>$A_{m} + \frac{F_m K_{ref} H_v}{H_i} (B_{m2} H_2 - B_{m1}) (C_{10} - 2E_{10}) - F_m (B_{eq1} + B_{eq2} H_2) [1 \ 0 \ 0]$</td>
</tr>
</tbody>
</table>

Corrected Table II:

<table>
<thead>
<tr>
<th>$A_{eq}$</th>
<th>$e^{A_{eq}(D_2 T_{-t_2} - t_2)} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} e^{A_{eq}(D_1 - 0.5) T} e^{A_{eq} D_2 T}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B_{eq1}$</td>
<td>$e^{A_{eq} D_2 T_{-t_2}} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} (A_{eq} - A_{01}) T e^{A_{eq}(D_1 - 0.5) T}$</td>
</tr>
<tr>
<td>$B_{eq2}$</td>
<td>$e^{A_{eq} D_2 T_{-t_2}} e^{A_{eq}(D_2 - 0.5) T} e^{A_{eq} D_1 T} (A_{eq} - A_{01}) T e^{A_{eq}(D_1 - 0.5) T}$</td>
</tr>
<tr>
<td>$B_m$</td>
<td>$A_{m} + \frac{F_m K_{ref} H_v}{H_i} (B_{m2} H_2 - B_{m1}) (C_{10} - 2E_{10}) - F_m (B_{eq1} + B_{eq2} H_2) [1 \ 0 \ 0]$</td>
</tr>
</tbody>
</table>

Fig. 9: Relation between individual switch duty with inductor current and control reference including the external ramp under digital peak CMC

obtained considering the timing diagram shown in Fig. 9. The perturbed duty ratios $\tilde{d}_1$ and $\tilde{d}_2$ of (8) can be expressed as

$$\tilde{d}_1 = F_m \left( \frac{1}{H_i} \tilde{i}_{ref,n} - \frac{1}{H_i} \tilde{i}_{LC,n} - \frac{1}{H_i} \tilde{i}_{L,n} \right)$$

$$\tilde{d}_2 = F_m \left( \frac{H_1}{H_i} \tilde{i}_{ref,n} - \frac{H_2}{H_i} \tilde{i}_{LC,n} - \frac{H_1}{H_i} \tilde{i}_{L,n} \right)$$

where, $F_m = 1/(m_1 + m_c)T$, $H_1 = (m_c - m_2)F_m T$, $H_2 = 1 - H_1$ and $m_c$ is the slope of compensating ramp. The perturbed duty ratios in (8) can be replaced by (9) and (10). By taking $m_1 = v_{in}/L$, $m_2 = (v_{in} - v_f)/L$, and $m_3 = (v_{in} + v_f - v_n)/L$, the DT SSM takes the form as

$$\tilde{x}_{n+1} = A_{m} \tilde{x}_n + B_{m} \tilde{i}_{ref},$$

where, the co-efficients $A_{m}$ and $B_{m}$ are defined in Table II. The DT control-to-output TF in a 3LFCB converter using peak CMC architecture can be expressed as

$$G_{vc}(z) = \tilde{v}_o(z)/\tilde{i}_{ref}(z) = C_{10} (2I - A_{m})^{-1} B_{m}$$

Using the parameters in Table I, $G_{vc}(z)$ can be expressed as

$$G_{vc}(z) = \frac{12.867(z - 0.8976)(z - 0.2242)}{(z - 0.9932)(z - 0.9)(z - 0.15)}$$

The frequency response of $G_{vc}(z)$ is compared with that obtained using SIMPLIS, which is shown in Fig. 6. As can be shown in the figure, both the magnitude and phase plots obtained using the analytical model in (13) and SIMPLIS are closely matching up to $1/5^{th}$ of the switching frequency $f_{sw}$.  

IV. THE PROPOSED HYBRID FRAMEWORK DESIGN AND STABILITY ANALYSIS OF DIGITAL CONTROLLER

A. Loop shaping using approximate CT boost converter model

Considering the approximate CT transfer function in (5), a type-II compensator, $G_c(s)$, is considered for the design of CMC [11], and the compensator takes the form as

$$G_c(s) = k_c \left( 1 + \frac{s}{\omega_{cz}} \right) / s \left( 1 + \frac{s}{\omega_{cp}} \right)$$

Consider $T_{loop}(s)$ as the CT closed loop TF under DCMC, which can be written as

$$T_{loop}(s) \approx k_g k_e H_v \frac{(1 - \frac{s}{\omega_{rhp}})(1 - \frac{s}{\omega_{lp}})}{s(1 + \frac{s}{\omega_{cp}})(1 + \frac{s}{\omega_{lp}})}$$

where the non-dominant zero due to ESR is neglected in the loop TF as $\omega_c \gg \omega_{rhp}$. A type-II compensator is designed following the steps similar to that in a boost converter [11], which can be summarized as follows.

1) Set zero, $\omega_{cz}$ of controller to cancel the dominant pole, $\omega_p$ of $G_{vc}(s)$
2) Set pole, $\omega_{cp}$ of controller in coincident with the RHP zero, $\omega_{rhp}$ of $G_{vc}(s)$
3) Set a controller pole at origin to eliminate steady-state error
4) Set dc gain, $k_c$ of controller as $k_c = \omega_c/(k_g H_v)$ to achieve the gain crossover frequency of $T_{loop}$ at $\omega_c$

Fig. 10: Frequency response of the uncompensated loop TF, compensator TF, and compensated loop TF of the 3LFCB converter under DCMC

The controller dc gain is selected to achieve the gain crossover frequency at $\omega_c = 0.25 \times \omega_{rhp}$. With the proposed controller design guidelines, using stable pole-zero cancellation, the compensator is designed and the frequency response of uncompensated loop TF ($T_{in,loop} = G_{vc} \times H_v$), compensator TF ($G_c$) and closed loop TF ($T_{loop}$) are potted in Fig. 10. The
closed loop stability is ensured for the designed compensator with a phase margin of 65° and gain margin of 14 dB. The analog controller is converted to a digital domain using the Backward difference formula for digital implementation, and the digital controller takes the form as

\[ G_c(z) \approx k'z(z - \alpha)/(z - 1)(z - \beta) \]  

where,
\[ k' = \frac{k_c\omega_c(1 + \omega_c)T}{\omega_c(1 + \omega_c)T}, \alpha = \frac{1}{1 + \omega_c T}, \text{and} \beta = \frac{1}{1 + \omega_c T} \]

The digital implementation of \( G_c(z) \) is shown in Fig. 11.

**B. Stability analysis from DT model**

The approximate CT model does not include the FC dynamics; consequently, it may not be able to predict fast-scale instability due to the FC voltage loop. On the other hand, the DT model can analytically predict stability boundaries for varying circuit and controller parameters as well as the effects due to the sampling delay and FC voltage loop.

![Fig. 11: Digital implementation of the controller, \( G_c(z) \)](image)

Fig. 11: Digital implementation of the controller, \( G_c(z) \)

**C. Simulation results with designed DT controller**

1) **Load transient response**

Using the DT output voltage controller defined in (16) and considering \( K_{pf} \) as 1, using SIMPLIS, the load transient performance of the 3LFCB converter is carried out for 1.25 A load step, which is shown in Fig. 16a. The parameter set is taken from Table-I. The figure indicates that the FC voltage is balanced at 200 V throughout the operation. Also, the output voltage settles with a settling time close to 1 ms with voltage undershoot/overshoot smaller than 1% of the rated output voltage during load transient.

2) **Reference voltage transient response**

A 20 V step change in output voltage reference is applied to verify the response to a reference voltage transient. The
inductor current and output voltage responses in SIMPLIS circuit simulation are shown in Fig. 16b. It can be seen that the output voltage is tracking the given reference voltage and settling at 380 V and 400 V, respectively, in 1 ms.

D. Summary of the hybrid controller design framework

The controller design steps of the 3LFCB converter start with the consideration of an approximate CT model of a CMC boost converter. A CT controller is designed by shaping the loop gain with stable pole-zero cancellation. The closed-loop bandwidth and stability margins are compared with the accurate DT model. The digital controller gains are obtained using a backward difference method. Using the DT models, the stability boundary is verified using the designed digital controller gains. These are further tuned to ensure desired closed-loop performance and stability of the 3LFCB converter, which are verified using SIMPLIS simulation. Using the proposed framework, fast transient performance and stable behavior are achieved for both load and reference step transients.

V. HARDWARE IMPLEMENTATION AND EXPERIMENTAL PERFORMANCE ANALYSIS

A. Hardware Setup

For the validation of the proposed DPCMC architecture, a hardware prototype of 3LFCB converter having scaled-down voltage and power level is developed, with converter specifications shown in Table III. The complete test setup is shown in Fig. 17. The details of key power stage components are provided in Table IV. The proposed digital current mode control is implemented using an FPGA device. The controller for the hardware specifications is redesigned using the same design steps defined in Section IV and is given by

$$G_c(z) = \frac{10.2(z - 0.952)}{(z - 1)(z - 0.41)}; \quad K_{pf} = 2$$ (18)

Table: Converter specifications used in Hardware prototype

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in} (V)</td>
<td>12</td>
</tr>
<tr>
<td>V_{o} (V)</td>
<td>48</td>
</tr>
<tr>
<td>f_{sw} (kHz)</td>
<td>100</td>
</tr>
<tr>
<td>P (W)</td>
<td>100</td>
</tr>
<tr>
<td>L (µH)</td>
<td>10</td>
</tr>
<tr>
<td>C_f (µF)</td>
<td>30</td>
</tr>
<tr>
<td>C_o (µF)</td>
<td>50</td>
</tr>
<tr>
<td>r_{on} (mΩ)</td>
<td>10</td>
</tr>
<tr>
<td>r_L (mΩ)</td>
<td>2.6</td>
</tr>
</tbody>
</table>

Table: Key components of hardware prototype

<table>
<thead>
<tr>
<th>Component</th>
<th>Part Number</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET</td>
<td>BSC0804LSATMA1</td>
<td>100V, 10.3 mΩ</td>
</tr>
<tr>
<td>Gate driver</td>
<td>LM5113DPRQR1</td>
<td>28ns propagation</td>
</tr>
<tr>
<td>Inductor</td>
<td>SER2918H-103KL</td>
<td>28A, 10 µH</td>
</tr>
<tr>
<td>Flying Capacitor</td>
<td>KRM55LR71H106KH01L</td>
<td>50V, 10 µF</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>KRM55WR72A156KH01L</td>
<td>100V, 15 µF</td>
</tr>
<tr>
<td>Input Capacitor</td>
<td>GCM32ER71E106KA57K</td>
<td>25V, 10 µF</td>
</tr>
<tr>
<td>Load Resistor</td>
<td>PWR263S-35-3000F</td>
<td>35W, 300 Ω</td>
</tr>
<tr>
<td>Current Sense Res.</td>
<td>CST0612-FC-R005E</td>
<td>1W, 5 mΩ</td>
</tr>
</tbody>
</table>

B. Steady-state performance

Fig. 18 shows the closed loop steady-state performance of the 3LFCB converter operating at 12 V input and 48 V output with a power rating of 40 W and switching frequency of
100 kHz. It is discussed in Section II-C that a ramp compensation is needed to stabilize the current loop at high-duty ratio operations, which can be seen in the control reference signal obtained using the proposed DCMC architecture in Fig. 2. The FC voltage balancing is achieved, which is shown in Fig. 18. The information related to the steady-state duty ratio and FC voltage can be extracted from the drain-to-source voltage waveform of the low-side MOSFET, $S_2$.

\[ V_{DS} = 12 \text{ V}, \quad v_{DS} = 48 \text{ V}, \quad f_{sw} = 100 \text{ kHz} \text{ and } R = 60 \Omega \]

![Fig. 18: Steady state result of 3LFCB converter under the proposed DCMC scheme with $v_{in} = 12 \text{ V}, v_{out} = 48 \text{ V}, f_{sw} = 100 \text{ kHz}$](image)

The efficiency analysis is carried out by varying the load current from 0.4A to 2.25A using a programmable electronic load (Chroma-63802) at 12 V input and 48 V output (regulated) with the switching frequency at 100 kHz. Both input, as well as output currents and voltages, are measured using KEITHLEY 2110 digital multi-meters, and the measured efficiency curve of the closed-loop 3LFCB converter is shown in Fig. 19. The efficiency calculation includes the driver losses and sensing circuit losses which are measured to be 0.25 W and 1.5 W respectively. The peak efficiency is found to be 96.75 % at the power output of 48 W.

![Fig. 19: Efficiency curve of 3LFCB converter under the proposed DCMC scheme with $v_{in} = 12 \text{ V}, v_{out} = 48 \text{ V},$ and $f_{sw} = 100 \text{ kHz}$](image)

The efficiency analysis is carried out by varying the load current from 0.4A to 2.25A using a programmable electronic load (Chroma-63802) at 12 V input and 48 V output (regulated) with the switching frequency at 100 kHz. Both input, as well as output currents and voltages, are measured using KEITHLEY 2110 digital multi-meters, and the measured efficiency curve of the closed-loop 3LFCB converter is shown in Fig. 19. The efficiency calculation includes the driver losses and sensing circuit losses which are measured to be 0.25 W and 1.5 W respectively. The peak efficiency is found to be 96.75 % at the power output of 48 W.

1) **Effect of FC voltage controller loop gain**

It is essential to verify closed-loop stability for the designed controller gains, particularly for investigating the effect of FC voltage loop gain. As discussed in Section IV-B, for the hardware specifications mentioned in Table III, it can be analytically shown that the converter experiences fast-scale instability for $K_{pf} > 9$. For validation, the FC voltage loop gain is set to $K_{pf} = 7$. The outer loop controller parameters of $G_c(z)$ are kept the same as defined in (18). It can be seen from Fig. 20a that the converter exhibits fast-scale instability, which is evident from the steady-state current ripple pattern. The closed-loop stability can be ensured by decreasing $K_{pf}$ to avoid any sub-harmonic instability. Hence, for the experimental results, a $K_{pf}$ of 2 is used.

![Fig. 20: Inductor current instability (a) with a higher FC voltage loop controller gain at $K_{pf} = 7$, keeping outer loop controller parameters constant (b) with a controller dc gain of 35 considering a sampling delay of $0.4 \times T$](image)

2) **Effect of voltage loop sampling delays**

The effect of the sampling delay on the closed-loop stability of the 3LFCB converter is discussed in Section IV-B. With the hardware specifications in Table III and with a sampling delay of $0.4 \times T$, fast-scale instability can be predicted for a controller dc gain higher than 44. Fig. 20b shows the hardware validation with inductor current experiencing instability for a controller dc gain of 35. This is primarily due to the sampling delay, which limits the upper boundary of the controller gain. Thus, the ADC latency should be considered to design the digital controller as the sampling delay sets the stability limit.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Analytical</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC voltage controller loop gain, $K_{pf}$</td>
<td>9</td>
<td>7</td>
</tr>
<tr>
<td>Output voltage controller dc gain</td>
<td>44</td>
<td>35</td>
</tr>
</tbody>
</table>

Table V summarizes the fast-scale instability boundaries of the controllers based on the DT model and experimental findings. Due to several unmodeled dynamics in the experimental prototypes, such as trace impedance, parasitic of power stage components, etc., the accuracy of analytical prediction cannot exactly match the experiment. However, a close agreement between the analytical predictions and experimental results is achieved. Thus, the developed DT model can be extended to high-power and multi-level converters in validating analytical predictions and experimental results with reasonable accuracy.

C. **Dynamic performance**

Experimental case studies related to both load and reference step transients are considered using the parameter set in Table III along with the digital Type-II (output) voltage controller and the FC voltage gain given by (18).

1) **Load Transient performance**

Fig. 21b shows hardware results of the load transient response for a step size of 0.96 A of the closed-loop controlled 3LFCB converter using the proposed digital CMC. The
figure shows that both the output voltage and FC voltage are regulated at 48 V and 24 V, respectively. The AC coupled enlarged response shows that for load step up/down transients, the output voltage takes 400 $\mu$s (40 switching cycles) to settle with less than 4% voltage undershoot/overshoot. The experimental load transient performance is found to be more or less consistent with the corresponding simulation result as tabulated in Table VI and illustrated in Fig. 21a. Also, the FC voltage is balanced throughout the load current range. While the performance can be improved by increasing the closed-loop bandwidth, this may result in large duty ratio perturbations during a transient recovery phase. In such cases, the first-order Taylor series expansion may not be accurate, and consequently, linear small-signal models may not be valid [11]. Further, at high load, the effect due to the RHP zero is severe, which makes it difficult to shape the closed-loop output impedance to achieve fast load transient performance.

2) Reference Transient performance

Reference transient response is crucial to evaluate closed-loop bandwidth in the presence of the RHP zero. From the output voltage trace in Fig. 22b, the settling time is nearly 600 $\mu$s (equivalent to 60 switching cycles) with 300 mV undershoot (1 V overshoot) during a reference step-down (step-up) transient. Table VI and Fig. 22a demonstrate that experimental reference transient performance is consistent with the simulation results.

Table VI: Performance comparison between simulation and hardware results

<table>
<thead>
<tr>
<th>Transient performance</th>
<th>Simulation</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load transient</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling time ($\mu$s)</td>
<td>340</td>
<td>400</td>
</tr>
<tr>
<td>Overshoot / undershoot (%)</td>
<td>1.25 / 0.8</td>
<td>2 / 0.6</td>
</tr>
<tr>
<td>Reference transient</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling time ($\mu$s)</td>
<td>560</td>
<td>600</td>
</tr>
<tr>
<td>Overshoot / undershoot (%)</td>
<td>1.25 / 0.8</td>
<td>2 / 0.6</td>
</tr>
</tbody>
</table>

A comparative study of SIMPLIS simulation and experimental results related to both load and reference transient responses are presented in Table VI. The simulated and experimental transient responses show close agreement. The minor difference can be attributed due to the presence of the unmodeled circuit dynamics.

A higher closed-loop bandwidth may be achievable by increasing the controller gain; however, this may lead to poor phase margin, resulting in higher output voltage undershoot/overshoot. Thus, it is necessary to make a trade-off between the gain crossover frequency and phase margin.
because of the existence of the RHP zero. Further, the effect due to the sampling delay may lead to fast-scale instability in the closed-loop 3LFCB converter. Interestingly, the proposed hybrid design framework is capable of accurately predicting the stability boundary using the proposed DT models and also provides useful guidelines for the digital controller design using the simplified CT small-signal models. Thus, the proposed framework is useful to design high-bandwidth stable digital controllers in multilevel DC-DC converters.

A comparative study of the proposed hybrid-design framework of 3LFCB converter with prior arts in terms of stability and performance is presented in Table VII. This work primarily contributes in designing stable and high-performance digital controllers for digitally controlled 3LFCB converters. These include a new DT analysis method to accurately predict fast-scale instability and a new hybrid design technique in simplifying the design of a digitally controlled 3LFCB converter, which has not been reported so far in the literature. Also, suitable design steps are presented for a suitable trade-off between closed-loop bandwidth and phase margin with stable cycle-by-cycle behavior in the presence of a RHP zero. The proposed DCMC is useful to achieve fast transient with the balanced FC voltage. In summary, many important stability and design aspects are presented in a digitally controlled 3LFCB converter, which were not presented earlier.

### VI. CONCLUSION

In this paper, a digital peak CMC architecture was proposed for fast transient and active FC balancing in a 3LFCB. A unified DT framework was developed to derive DT large and small-signal models of a 3LFCB converter under the proposed DCMC architecture. A hybrid design framework was proposed by combining CT and DT models to retain design simplicity and accuracy to predict fast scale instability. A 100 W, 12/48 V 3LFCB converter prototype was developed, and the proposed modeling and design techniques were validated. The proposed DCMC architecture in combination with the proposed hybrid design method could achieve fast load as well as reference transient performance with stable periodic behavior and active FC balancing. The proposed design framework can be extended to other digital control techniques to design high-performance stable multilevel DC-DC converters.

### REFERENCES


### TABLE VII: Performance and stability comparative analysis of the proposed hybrid-design framework with prior arts

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware specifications</td>
<td>168V/400V, 3kW, 50kHz</td>
<td>80V/200V, 400W, 40kHz</td>
<td>215V/600V, 1.5kW, 18kHz</td>
<td>375/5V, 0.4W, 0.5–45MHz (CMOS)</td>
<td>12V/48V, 100W, 100kHz</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>98.3%</td>
<td>Not reported</td>
<td>96.8%</td>
<td>96.75%</td>
<td></td>
</tr>
<tr>
<td>Modeling technique</td>
<td>CT SSM</td>
<td>CT SSM</td>
<td>CT SSM</td>
<td>Not reported</td>
<td>DCMC (Large + small signal)</td>
</tr>
<tr>
<td>Control implementation</td>
<td>VMC with MPPT</td>
<td>Digital VMC</td>
<td>DCMC</td>
<td>ACC-PFM control</td>
<td>DCMC</td>
</tr>
<tr>
<td>Controller design steps</td>
<td>Provided</td>
<td>Provided</td>
<td>Not reported</td>
<td>Detailed guidelines provided</td>
<td></td>
</tr>
<tr>
<td>Fast-scale stability boundary</td>
<td>Not reported</td>
<td>Identified analytically and experimentally</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


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